library IEEE;

use IEEE.STD\_LOGIC\_ARITH.ALL;

use IEEE.STD\_LOGIC\_UNSIGNED.ALL;

use IEEE.STD\_LOGIC\_1164.ALL;

entity fourbitcounter is

port( Number: in std\_logic\_vector(0 to 3);

rst: in std\_logic;

dr: in std\_logic;

clk: in std\_logic;

Ld: in std\_logic;

output: out std\_logic\_vector(0 to 3) );

end fourbitcounter;

architecture Behavioral of fourbitcounter is

signal temp: std\_logic\_vector(0 to 3);

begin

process(clk,rst)

begin

if rst='1' then

temp <= "0000";

elsif ( clk'event and clk='1') then

if Ld='1' then

temp <= Number;

elsif (Ld='0' and dr='0') then

temp <= temp + 1;

elsif (Ld='0' and dr='1') then

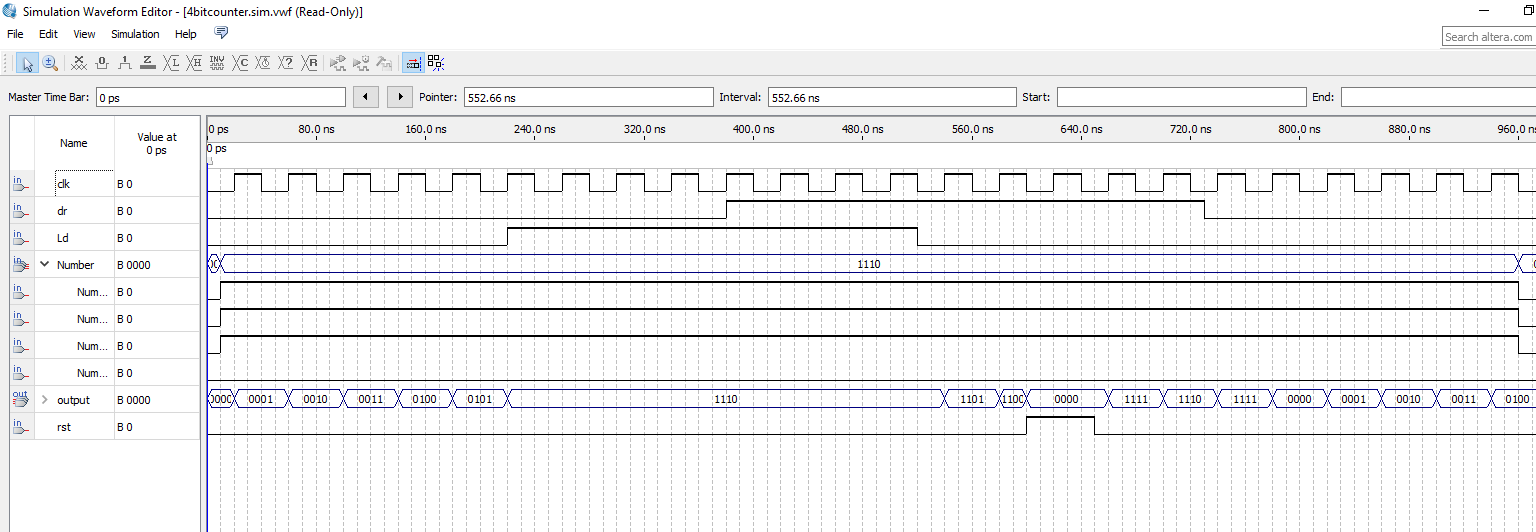
temp <= temp - 1;

end if;

end if;

end process;

output <= temp;

end Behavioral;